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Patent Document Report

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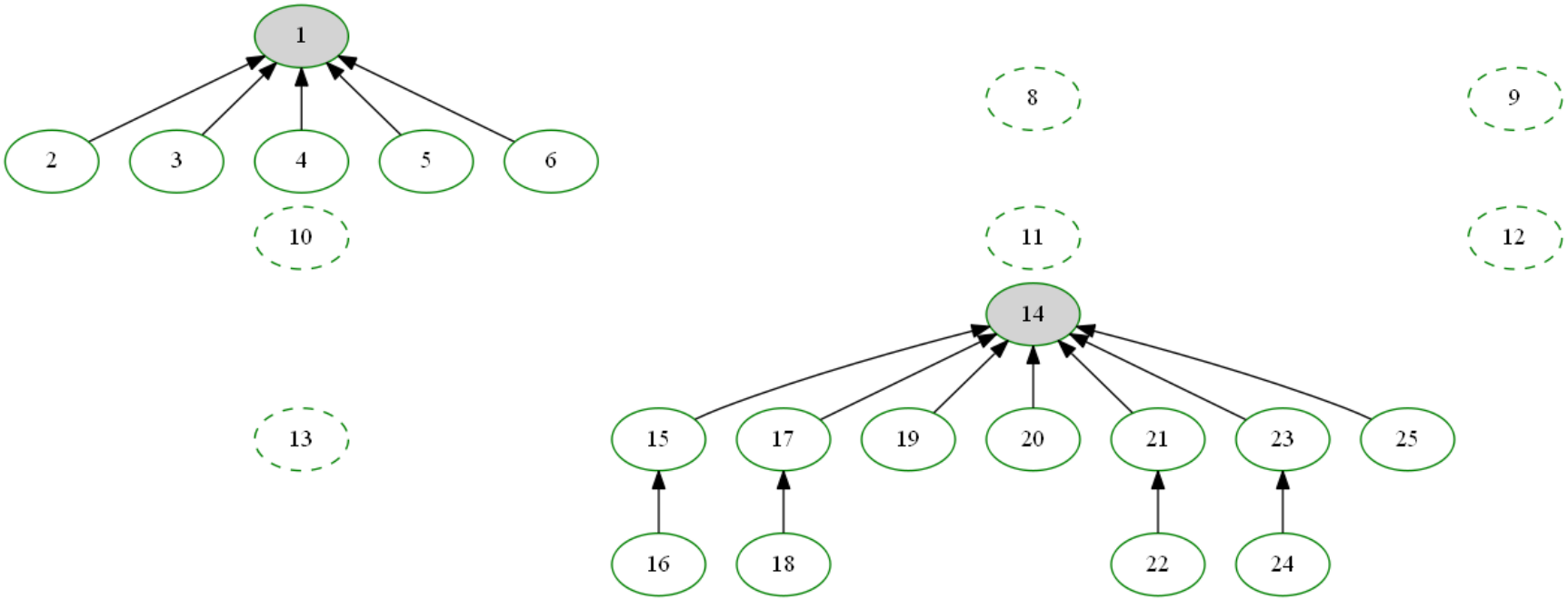
I. Claims (Tree and Text)

Note: *The type of each claim is indicated by its color.*[1] *Independent claims are grey inside. Claims with invalid parent numbers are dotted. If present, status indicators will be provided in brackets next to the claim numbers.*[2]



1. A method for forming a liquid crystal display including a thin film transistor, said method comprising the steps of:

depositing a first metal layer on a substrate;

depositing a second metal layer on said first metal layer opposite said substrate;

patterning said first and second metal layers to provide a gate electrode on a TFT area of said substrate and to provide a gate pad on a pad area of said substrate;

forming an insulating layer on said gate electrode and on said gate pad, and on said substrate;

[1] Claim type color legend: **Method/process**; **Apparatus/device**; **Composition**; **Article of manufacture**; **112(6)**; **Product by process**; **Jepson**

[2] Status indicator legend: **[O]**="Original"; **[PP]**="Previously Presented"; **[CA]**="Currently Amended"; **[N]**="New"; **[X]**="Cancelled"; **[W]**="Withdrawn"; **[WA]**="Withdrawn and Amended"; **[NE]**="Not Entered"

forming a semiconductor layer on said insulating layer opposite said gate electrode wherein said semiconductor layer includes a channel region opposite said gate electrode and first and second spaced apart source/drain regions separated by said channel region; forming first and second spaced apart metal source/drain electrodes on said respective first and second spaced apart semiconductor source/drain regions; forming a protective layer on said exposed portion of said first semiconductor layer opposite said substrate, on said first and second metal source/drain electrodes opposite said substrate, and on said insulating layer opposite said gate pad; forming a first contact hole in said protective layer exposing a portion of one of said source/drain electrodes; forming a second contact hole in said protective layer and said insulating layer exposing a portion of said gate pad wherein said second contact hole exposes only a surface portion of said gate pad opposite said substrate; forming a transparent conductive layer on said protective layer opposite said substrate; and patterning said transparent conductive layer to form a pixel electrode electrically connected to said exposed portion of said source/drain electrode and to said exposed portion of said gate pad.
2. A method according to claim 1 wherein said first metal layer comprises a material chosen from the group consisting of aluminum and an aluminum alloy.
3. A method according to claim 1 wherein said second metal layer comprises a refractory metal.
4. A method according to claim 1 wherein said pixel electrode covers said exposed surface portion of said gate pad and extends onto said protective layer adjacent said second contact hole.
5. A method according to claim 1 wherein said step of forming said semiconductor layer comprises forming a semiconductor layer portion on said insulating layer opposite said pad area of said substrate so that said semiconductor layer portion is adjacent said second contact hole.
6. A method according to claim 1 wherein said step of forming said metal source/drain electrodes comprises forming a metal layer portion on said insulating layer opposite said pad area of said substrate so that said metal layer portion is adjacent said second contact hole.
14. A method for forming a liquid crystal display, said method comprising the steps of: forming a first metal layer on a substrate; patterning said first metal layer to provide a gate electrode on a TFT area of said substrate and to provide a gate pad on a pad area of said substrate; forming an insulating layer on said gate electrode and on said gate pad; forming a patterned semiconductor layer on said insulating layer opposite said gate electrode and opposite said gate pad; forming a second patterned metal layer on said semiconductor layer opposite said insulating layer; forming a transparent conductive layer on said second patterned metal layer and on said insulating layer opposite said substrate; and

patterning said transparent conductive layer, said second patterned metal layer, and said patterned semiconductor layer to provide a data line, metal source/drain electrodes, and a pixel electrode.
15. A method according to claim 14 further comprising the steps of: forming a protective layer on said substrate covering said data line, said source/drain electrodes, and said pixel electrode; and patterning said protective layer to expose portions of said pixel electrode.
16. A method according to claim 15 wherein said step of patterning said protective layer comprises forming a black photoresist mask, and wherein said black photoresist mask is maintained on said protective layer thereby providing a black matrix.
17. A method according to claim 14 wherein said semiconductor layer includes a first amorphous silicon layer and a second doped amorphous silicon layer on said first amorphous silicon layer opposite said substrate.
18. A method according to claim 17 wherein said step of patterning said semiconductor layer comprises etching a portion of said second doped amorphous silicon layer between said source/drain electrodes.
19. A method according to claim 14 wherein said first metal layer comprises a material selected from the group consisting of Aluminum, an Aluminum alloy, and a refractory metal.
20. A method according to claim 14 wherein said first metal layer includes a first sub-layer comprising a refractory metal, and a second sub-layer comprising a material chosen from the group consisting of Aluminum and an Aluminum alloy.
21. A method according to claim 14 wherein said first metal layer includes a first sub-layer comprising a refractory metal on said substrate and a second sub-layer comprising a material chosen from the group consisting of Aluminum and an Aluminum alloy on said first sub-layer opposite said substrate.
22. A method according to claim 21 wherein said refractory metal selected from the group consisting of chromium (Cr), Molybdenum (Mo), Titanium (Ti), and Tantalum (Ta).
23. A method according to claim 14 wherein said first metal layer includes a first sub-layer comprising a material chosen from the group consisting of Aluminum and an Aluminum alloy on said substrate and a second sub-layer comprising a refractory metal on said first sub-layer opposite said substrate.
24. A method according to claim 23 wherein said refractory metal selected from the group consisting of chromium (Cr), Molybdenum (Mo), Titanium (Ti), and Tantalum (Ta).
25. A method according to claim 14 further comprising the step of removing a portion of said second sub-layer from said gate pad.
8. A method according to claim 7 wherein said first metal layer comprises a refractory metal.
9. A method according to claim 7 wherein said second metal layer comprises a material chosen from the group consisting of Aluminum and an Aluminum alloy.

10. A method according to claim 7 wherein said pixel electrode covers said exposed surface portion of said gate pad and said substrate adjacent said gate pad, and wherein said pixel electrode extends onto said protective layer adjacent said second contact hole.
11. A method according to claim 7 wherein said step of forming said semiconductor layer comprises forming a semiconductor layer portion on said insulating layer opposite said pad area of said substrate so that said semiconductor layer portion is adjacent said second contact hole.
12. A method according to claim 7 wherein said step of forming said metal source/drain electrodes comprises forming a metal layer portion on said insulating layer opposite said pad area of said substrate so that said metal layer portion is adjacent said second contact hole.
13. A method according to claim 7 wherein said step of patterning said first and second metal layers comprises providing a plurality of interconnections on said pad area of said substrate wherein said interconnections are connected to said gate pad.

II. Claim Language Errors/Warnings

Claim	Error/Warning Message	Suggested Fix
8. A method according to claim 7 wherein said first metal layer comprises a refractory metal.	***Error:*** Claim number is out of sequence.	Make sure claims are numbered sequentially. See MPEP 608.01(j)
	Error: Claim depends from an invalid parent.	Make sure the claim references an existing parent claim that is not cancelled.
9. A method according to claim 7 wherein said second metal layer comprises a material chosen from the group consisting of Aluminum and an Aluminum alloy.	***Error:*** Claim depends from an invalid parent.	Make sure the claim references an existing parent claim that is not cancelled.
10. A method according to claim 7 wherein said pixel electrode covers said exposed surface portion of said gate pad and said substrate adjacent said gate pad, and wherein said pixel electrode extends onto said protective layer adjacent said second contact hole.	***Error:*** Claim depends from an invalid parent.	Make sure the claim references an existing parent claim that is not cancelled.
11. A method according to claim 7 wherein said step of forming said semiconductor layer comprises forming a semiconductor layer portion on said insulating layer opposite said pad area of said substrate so that said semiconductor layer portion is adjacent said second contact hole.	***Error:*** Claim depends from an invalid parent.	Make sure the claim references an existing parent claim that is not cancelled.

Claim	Error/Warning Message	Suggested Fix
12. A method according to claim 7 wherein said step of forming said metal source/drain electrodes comprises forming a metal layer portion on said insulating layer opposite said pad area of said substrate so that said metal layer portion is adjacent said second contact hole.	***Error:*** Claim depends from an invalid parent.	Make sure the claim references an existing parent claim that is not cancelled.
13. A method according to claim 7 wherein said step of patterning said first and second metal layers comprises providing a plurality of interconnections on said pad area of said substrate wherein said interconnections are connected to said gate pad.	***Error:*** Claim depends from an invalid parent.	Make sure the claim references an existing parent claim that is not cancelled.

III. **Antecedents Errors/Warnings**[3]

Claim	Error/Warning
1. A method for forming a liquid crystal display including a thin film transistor, said method comprising the steps of:	{1} ***No antecedent:*** "said exposed portion."
	{2} ***No antecedent:*** "said first semiconductor layer."
depositing a first metal layer on a substrate;	{3} ***Double-check:*** "said first metal source / drain electrode." Is "first spaced apart metal source / drain electrode" in claim 1 the proper antecedent reference for this term?
depositing a second metal layer on said first metal layer opposite said substrate;	
patterning said first and second metal layers to provide a gate electrode on a TFT area of said substrate and to provide a gate pad on a pad area of said substrate;	{4} ***Double-check:*** "said second metal source / drain electrode." Is "second spaced apart metal source / drain electrode" in claim 1 the proper antecedent reference for this term?
forming an insulating layer on said gate electrode and on said gate pad, and on said substrate;	{5} ***Double-check:*** "said source / drain electrodes." Is "first spaced apart metal source / drain electrode" in claim 1 the proper antecedent reference for this term?
forming a semiconductor layer on said insulating layer opposite said gate electrode wherein said semiconductor layer includes a channel region opposite said gate electrode and first and second spaced apart source/drain regions separated by said channel region;	{6} ***Double-check:*** "said source / drain electrode." Is "first spaced apart metal source / drain electrode" in claim 1 the proper antecedent reference for this term?
forming first and second spaced apart metal source/drain electrodes on said respective first and second spaced apart semiconductor source/drain regions;	
forming a protective layer on *said exposed portion{1}* of *said first semiconductor layer{2}* opposite said substrate, on *said first and second metal source/drain electrode{3}{4}*s opposite said substrate, and on said insulating layer opposite said gate pad;	
forming a first contact hole in said protective layer exposing a portion of one of	

[3] Deleted (i.e., stricken-through) claim text, if any, is not shown.

Claim	Error/Warning
said source/drain electrodes{5}; forming a second contact hole in said protective layer and said insulating layer exposing a portion of said gate pad wherein said second contact hole exposes only a surface portion of said gate pad opposite said substrate; forming a transparent conductive layer on said protective layer opposite said substrate; and patterning said transparent conductive layer to form a pixel electrode electrically connected to said exposed portion of *said source/drain electrode{6}* and to said exposed portion of said gate pad.	
4. A method according to claim 1 wherein *said pixel electrode covers{1} said exposed surface portion{2}* of said gate pad and extends onto said protective layer adjacent said second contact hole.	{1} ***No antecedent:*** "said pixel electrode covers." {2} ***Double-check:*** "said exposed surface portion." Is "exposes only a surface portion" in claim 1 the proper antecedent reference for this term?
6. A method according to claim 1 wherein said step of forming *said metal source/drain electrodes* comprises forming a metal layer portion on said insulating layer opposite said pad area of said substrate so that said metal layer portion is adjacent said second contact hole.	***Double-check:*** "said metal source / drain electrodes." Is "first spaced apart metal source / drain electrode" in claim 1 the proper antecedent reference for this term?
8. A method according to claim 7 wherein *said first metal layer* comprises a refractory metal.	***No antecedent:*** "said first metal layer."

Claim	Error/Warning
9. A method according to claim 7 wherein *said second metal layer* comprises a material chosen from the group consisting of Aluminum and an Aluminum alloy.	***No antecedent:*** "said second metal layer."
10. A method according to claim 7 wherein *said pixel electrode covers{1} said exposed surface portion{2}* of *said gate pad{3}* and *said substrate{4}* adjacent said gate pad, and wherein *said pixel electrode{5}* extends onto *said protective layer{6}* adjacent *said second contact hole{7}*.	{1} ***No antecedent:*** "said pixel electrode covers." {2} ***No antecedent:*** "said exposed surface portion." {3} ***No antecedent:*** "said gate pad." {4} ***No antecedent:*** "said substrate." {5} ***No antecedent:*** "said pixel electrode." {6} ***No antecedent:*** "said protective layer." {7} ***No antecedent:*** "said second contact hole."
11. A method according to claim 7 wherein said step of forming *said semiconductor layer{1}* comprises forming a semiconductor layer portion on *said insulating layer{2}* opposite *said pad area{3}* of *said substrate{4}* so that said semiconductor layer portion is adjacent *said second contact hole{5}*.	{1} ***No antecedent:*** "said semiconductor layer." {2} ***No antecedent:*** "said insulating layer." {3} ***No antecedent:*** "said pad area." {4} ***No antecedent:*** "said substrate." {5} ***No antecedent:*** "said second contact hole."
12. A method according to claim 7 wherein said step of forming *said metal source/drain electrodes{1}* comprises forming a metal layer portion on *said insulating layer{2}* opposite *said pad area{3}* of *said substrate{4}* so that said metal layer portion is adjacent *said second contact hole{5}*.	{1} ***No antecedent:*** "said metal source / drain electrodes." {2} ***No antecedent:*** "said insulating layer." {3} ***No antecedent:*** "said pad area." {4} ***No antecedent:*** "said substrate." {5} ***No antecedent:*** "said second contact hole."
13. A method according to claim 7 wherein said step of patterning *said first and second metal layer{1}{2}*s comprises providing a plurality of interconnections on *said pad area{3}* of *said substrate{4}* wherein said	{1} ***No antecedent:*** "said first metal layer." {2} ***No antecedent:*** "said second metal layer." {3} ***No antecedent:*** "said pad area."

Claim	Error/Warning
interconnections are connected to *said gate pad{5}*.	{4} ***No antecedent:*** "said substrate." {5} ***No antecedent:*** "said gate pad."
14. A method for forming a liquid crystal display, said method comprising the steps of: forming a first metal layer on a substrate; patterning said first metal layer to provide a gate electrode on a TFT area of said substrate and to provide a gate pad on a pad area of said substrate; forming an insulating layer on said gate electrode and on said gate pad; forming a patterned semiconductor layer on said insulating layer opposite said gate electrode and opposite said gate pad; forming a second patterned metal layer on *said semiconductor layer* opposite said insulating layer; forming a transparent conductive layer on said second patterned metal layer and on said insulating layer opposite said substrate; and patterning said transparent conductive layer, said second patterned metal layer, and said patterned semiconductor layer to provide a data line, metal source/drain electrodes, and a pixel electrode.	***Double-check:*** "said semiconductor layer." Is "a patterned semiconductor layer" in claim 14 the proper antecedent reference for this term?
15. A method according to claim 14 further comprising the steps of: forming a protective layer on said substrate covering said data line, *said*	***Double-check:*** "said source / drain electrodes." Is "metal source / drain electrodes" in claim 14 the proper antecedent reference for this term?

Claim	Error/Warning
source/drain electrodes, and said pixel electrode; and patterning said protective layer to expose portions of said pixel electrode.	
17. A method according to claim 14 wherein *said semiconductor layer* includes a first amorphous silicon layer and a second doped amorphous silicon layer on said first amorphous silicon layer opposite said substrate.	***Double-check:*** "said semiconductor layer." Is "a patterned semiconductor layer" in claim 14 the proper antecedent reference for this term?
18. A method according to claim 17 wherein said step of patterning *said semiconductor layer{1}* comprises etching a portion of said second doped amorphous silicon layer between *said source/drain electrodes{2}*.	{1} ***Double-check:*** "said semiconductor layer." Is "a patterned semiconductor layer" in claim 14 the proper antecedent reference for this term?
	{2} ***Double-check:*** "said source / drain electrodes." Is "metal source / drain electrodes" in claim 14 the proper antecedent reference for this term?
25. A method according to claim 14 further comprising the step of removing a portion of *said second sub-layer* from said gate pad.	***No antecedent:*** "said second sub - layer."

IV. Claim Terms without Explicit Support in the Specification

Claim	Term Without Support
10. A method according to claim 7 wherein said pixel electrode covers said exposed surface portion of said gate pad and said substrate adjacent said gate pad, and wherein said pixel electrode extends onto said protective layer adjacent said second contact hole.	pixel electrode covers
13. A method according to claim 7 wherein said step of patterning said first and second metal layers comprises providing a plurality of interconnections on said pad area of said substrate wherein said interconnections are connected to said gate pad.	interconnections
4. A method according to claim 1 wherein said pixel electrode covers said exposed surface portion of said gate pad and extends onto said protective layer adjacent said second contact hole.	pixel electrode covers
16. A method according to claim 15 wherein said step of patterning said protective layer comprises forming a black photoresist mask, and wherein said black photoresist mask is maintained on said protective layer thereby providing a black matrix.	black photoresist mask black matrix
20. A method according to claim 14 wherein said first metal layer includes a first sub-layer comprising a refractory metal, and a second sub-layer comprising a material chosen from the group consisting of Aluminum and an Aluminum alloy.	sub-layer

Claim	Term Without Support
21. A method according to claim 14 wherein said first metal layer includes a first sub-layer comprising a refractory metal on said substrate and a second sub-layer comprising a material chosen from the group consisting of Aluminum and an Aluminum alloy on said first sub-layer opposite said substrate.	sub-layer
23. A method according to claim 14 wherein said first metal layer includes a first sub-layer comprising a material chosen from the group consisting of Aluminum and an Aluminum alloy on said substrate and a second sub-layer comprising a refractory metal on said first sub-layer opposite said substrate.	sub-layer
25. A method according to claim 14 further comprising the step of removing a portion of said second sub-layer from said gate pad.	sub-layer
22. A method according to claim 21 wherein said refractory metal selected from the group consisting of chromium (Cr), Molybdenum (Mo), Titanium (Ti), and Tantalum (Ta).	tantalum
24. A method according to claim 23 wherein said refractory metal selected from the group consisting of chromium (Cr), Molybdenum (Mo), Titanium (Ti), and Tantalum (Ta).	tantalum

V. Inconsistent Part Names/Numbers

Note: *terms completely in red are more likely to be incorrectly named or numbered. With partially inconsistent names, mismatched sections are colored in orange.*

Part Number	Consistently Used Part Name [# of occurrences]	Inconsistently Named/Numbered Part [# of occurrences]	Citations [Page/Line # in the document]
3	**source lines**	data lines	Also, a **plurality of data lines 3** are provided lengthwise, and a respective data pad 4 is provided ... [Page 13, line 16.]
10	**substrate**	transparent line	A metal layer is forming by depositing aluminum (Al) on a **transparent line 10**, and this metal layer is patterned using a first photolithography step to ... [Page 6, line 6.]
11	**gate electrode [4]**	gate line	An insulating layer 15, such as a nitride layer, is deposited on the substrate 10 including the **gate line 11** and the anodic oxide layer 13. [Page 6, line 13.]
21a	**drain electrodes**	source electrode	A **source electrode 21a** and a drain electrode 21b are formed on the TFT are of the ... [Page 6, line 21.]
32	**first metal layer**	second metal layers	2 formed on the TFT and pad areas of the substrate have a double layer structure formed by sequentially depositing first and **second metal layers 32** and 34. [Page 7, line 26.]
		aluminum alloy layer	As shown, this TFT-LCD includes a substrate 30, an **aluminum alloy layer 32**, a refractory metal capping layer 34, an insulating layer 36 ... [Page 7, line 20.]
34	**second metal layer [3]**	refractory metal capping layer	As shown, this TFT-LCD includes a substrate 30, an aluminum alloy layer 32, a **refractory metal capping layer 34**, an insulating layer 36 which can be a nitride layer... [Page 7, line 21.]

Part Number	Consistently Used Part Name [# of occurrences]	Inconsistently Named/Numbered Part [# of occurrences]	Citations [Page/Line # in the document]
51	**first metal layer [2]**	second metal layers	On the pad area of the substrate, the gate electrode (including the first and **second metal layers 51** and 53) and the pad electrode 61c are connected by the ... [Page 8, line 18.]
70	**substrate [2]**	transparent substrate	7A, a first metal layer 72 is formed by depositing Al or an Al alloy on a **transparent substrate 70**. [Page 13, line 36.]
72	**first metal layer [3]**	layers	This ITO layer is patterned using fifth photolithography and etch steps to provide a pixel electrode 86 connected to the gate pad including **layers 72** and 74 on the pad area of the substrate and connected to the drain ... [Page 15, line 1.]
74	**second metal layer [3]**	layers	This ITO layer is patterned using fifth photolithography and etch steps to provide a pixel electrode 86 connected to the gate pad including **layers 72 and 74** on the pad area of the substrate and connected to the drain ... [Page 15, line 1.]
78	**amorphous silicon layer [2]**	layers [2]	7C, a third metal layer is formed by depositing a metal such as chromium (Cr), molybdenum (Mo), or titanium (Ti) on the patterned semiconductor layer including **layers 78** and 80 opposite the substrate 70. [Page 14, line 12.] Next, after forming a semiconductor layer comprising an amorphous silicon layer 78 and a doped amorphous silicon layer on the insulating layer 76, a patterned semiconductor layer including **layers 78** and 80 is formed on the TFT area of the substrate by performing a ... [Page 14, line 8.]
80	**layers [2]**	doped amorphous silicon	At this time, the **doped amorphous silicon layer 80** is also etched to expose a portion of the amorphous silicon ... [Page 14, line 15.]

Part Number	Consistently Used Part Name [# of occurrences]	Inconsistently Named/Numbered Part [# of occurrences]	Citations [Page/Line # in the document]
		layer	
112	**pixel electrode**	gate pad	At this time, a portion of the protective layer 124 on the pixel electrode 112 is etched and the protective layer 124 and insulating layer 114 on the **gate pad 112** are partially etched so that a portion of the pad electrode is exposed... [Page 16, line 5.]

VI. **Inconsistent Part Numbers in Figures**

Part Number	Found in Figures?	Found in Specification?
1	No	Yes
2	No	Yes
3	No	Yes
4	No	Yes
10	No	Yes
11	No	Yes
13	No	Yes
15	No	Yes
17	No	Yes
19	No	Yes
110	No	Yes
111	Yes	No
112	No	Yes
114	No	Yes
124	No	Yes
125	No	Yes
21a	No	Yes
21b	No	Yes
21c	No	Yes
22	No	Yes
23	No	Yes
25	No	Yes
222	Yes	No
2b	No	Yes
30	No	Yes
32	No	Yes
34	No	Yes
36	No	Yes

38	No	Yes
333	Yes	No
40a	No	Yes
42a	No	Yes
42b	No	Yes
5	No	Yes
6	No	Yes
44	No	Yes
46	No	Yes
50	No	Yes
51	No	Yes
53	No	Yes
55	No	Yes
57	No	Yes
59	No	Yes
61a	No	Yes
61b	No	Yes
61c	No	Yes
63	No	Yes
67	No	Yes
70	No	Yes
72	No	Yes
74	No	Yes
76	No	Yes
78	No	Yes
80	No	Yes
84	No	Yes
86	No	Yes
88	No	Yes
444	Yes	No
555	Yes [multiple appearances]	No
82a	No	Yes

82b	**No**	**Yes**
890a	**Yes [multiple appearances]**	**No**